What is claimed is:

1. A signal communication apparatus of the clock reproduction transmission type whereby communication is conducted using parallel optical or electrical signals, the apparatus comprising a data signal reception unit for receiving transmitted data signals, said data signal reception unit comprising:

a clock signal extraction/selection circuit for selecting a number b of bits from a-bit data signals in n-bit data signals that have been received, where a is an integer such that $2 \leq a < n$, and where b is an integer such that $1 \leq b \leq a$, extracting a clock signal from the selected data signal, and outputting the extracted clock signal as a reference clock signal;

a number n of phase adjusting circuits for adjusting the phase of the reference clock signal and for producing reproduction clock signals for each of the received n-bit data signals, the reproduction clock signal providing the timing for redigitization of each data signal; and

a sampling means for redigitizing each of the received n-bit data signals in accordance with the timing provided by the reproduction clock signal for each bit.

2. The signal communication apparatus according to claim 1, wherein the clock signal extraction/selection means comprises:

a first function sections provided for each of the a-bit data signals of the received n-bit data signals, the first function sections constituting a part of a clock signal extraction function;

a selection means for selecting b of the a first function sections; and

b second function sections constituting the rest of the clock extraction function and being adapted to output the reference clock signal based on the outputs of the b first function sections.

3. The signal communication apparatus according to claim 2, wherein the first

function section comprises *a* phase comparators for comparing the phase of the *a*-bit data signals of the received *n*-bit data signals with that of the reference clock signal, and wherein the second function section comprises *b* loop filters and *b* voltage controlled oscillators to which the outputs of the *b* phase comparators selected by the selection means are fed.

4. The signal communication apparatus according to claim 1, wherein the clock signal extraction/selection circuit is provided for each of *a* blocks of the received *n*-bit data signals, and

the reference clock signal outputted by the clock signal extraction/selection circuit for each block is distributed to phase adjusting circuits in the block,

wherein the clock signal extraction/selection circuit comprises a circuit for switching the reference clock signal, wherein, in case an abnormality develops in a data signal bit being used for extracting the reference clock signal for a block and so the clock signals cannot be correctly extracted, the reference clock signal for the block with the abnormality is switched by the switching circuit to a reference clock signal extracted from another block.

5. The signal communication apparatus according to claim 1, further comprising an input terminal for a selection signal for changing the selection of the *a* bits in the clock signal extraction/selection circuit.

6. The signal communication apparatus according to claim 1, further comprising a clock signal monitoring circuit that monitors the voltage level or frequency of the clock signal extracted from the reference clock signal or data signal and which, if it detects abnormality in the voltage level or frequency, outputs a control signal for switching the reference clock signal to a normal clock signal extracted from a different data signal bit.

7. The signal communication apparatus according to claim 6, further comprising an alarm means for indicating the occurrence of an abnormality in the event of detection of an abnormality by the clock signal monitoring circuit.

8. The signal communication apparatus according to claim 1, further comprising a data signal monitoring circuit that monitors at least one kind of information about the communication quality of the data signal from which the clock signal is to be extracted, the information being selected from the group consisting of voltage level, rise and fall edges, presence or absence of bit error, bit error ratio, and the amount of jitter.

9. The signal communication apparatus according to claim 8, further comprising an alarm means for indicating the occurrence of an abnormality in the event that the data signal monitoring circuit detects an abnormality.

10. The signal communication apparatus according to claim 1, further comprising a data signal monitoring circuit that monitors at least one kind of information about the communication quality of the redigitized *n*-bit data signals, the information being selected from the group consisting of voltage level, presence or absence of bit error, bit error ratio, and the amount of jitter, wherein, if the information about the communication quality exceeds a predetermined tolerance value, the monitoring circuit deems the relevant bit unfit for communication and produces a data signal abnormality notifying signal.

11. The signal communication apparatus according to claim 9 further comprising a circuit for determining a normally operable data signal bit based on the data signal abnormality notifying signal, and outputting a bit routing control signal designating the manner of routing the data signals to the individual bits.

12. The signal communication apparatus according to claim 11, further comprising an output circuit for sending the bit routing control signal to the signal communication apparatus from which the data signals have been received.

13. The signal communication apparatus according to claim 12, further comprising a circuit for restoring the data signals of each bit back to the original order of data based on the bit routing control signal.

14. A signal communication apparatus of the clock reproduction transmission type in which communication is conducted using parallel optical or electric signals, the apparatus comprising a data signal reception section for receiving data signals that have been transmitted, wherein the data signal reception section comprises:

a clock signal extraction circuit for extracting a clock signal from each of a-bit data signals in n-bit data signals that have been received, where a is an integer such that $2 \leq a < n$;

a clock signal selection circuit for selecting a single clock signal from the extracted a clock signals, the clock signal being designated as a reference clock signal; and

a number n of phase adjusting circuits for adjusting the phase of the selected reference clock signal to produce a reproduction clock signal for each bit, the reproduction clock signal providing the timing of redigitization of each of the received n-bit data signals.

15. A signal communication apparatus of the clock reproduction transmission type in which communication is conducted using parallel optical or electric signals, the apparatus comprising a data signal reception section for receiving data signals that have been transmitted, wherein the data signal reception section comprises:

a data signal selection circuit for selecting a single data signal from a-bit

data signals in n-bit data signals that have been received, where a is an integer such that $2 \leq a < n$;

a clock signal extraction circuit for extracting a clock signal from the selected data sign; and

a number n of phase adjusting circuits for adjusting the phase of the extracted reference clock signal to produce a reproduction clock signal for each bit, the reproduction clock signal providing the timing of redigitization of each of the received n-bit data signals.

16. A signal communication system of the clock reproduction transmission type in which communication is conducted using parallel optical or electric signals, the system comprising:

a data signal transmission section for transmitting parallel data signals; and

a data signal reception section for receiving the parallel data signals that have been transmitted, wherein

the data signal reception section comprises:

a clock signal extraction/selection circuit for selecting a number b of bits from a number a of bits in n-bit data signals that have been received, where a is an integer such that $2 \leq a < n$, and b is such an integer that $1 \leq b \leq a$, the clock signal extraction/selection circuit extracting a clock signal from the selected data signal and outputting it as a reference clock signal;

a number n of phase adjusting circuits for adjusting the phase of the reference clock signal to generate a reproduction clock signal for each bit, the reproduction clock signal providing the timing of redigitizing each of the n-bit data signals that have been received;

a sampling means for redigitizing each of the received n-bit data signals using the timing provided by the reproduction clock signal for each bit;

a monitoring means for monitoring each of the n-bit data signals obtained from the sampling means in terms of whether or not the data is normal; and

a data signal bit control circuit that determines the usability of the n-bit data signals in accordance with the output of the monitoring means, produces a routing control signal for routing a row of data only to normally operable data signal bits, and transmits the routing control signal to the data signal transmission section, and wherein

the data signal transmission section comprises:

an input circuit for receiving the bit routing control signal transmitted from the data signal bit control circuit in the data signal reception section; and

a routing circuit for routing a row of data to be transmitted to the normally operable data signal bits in accordance with the bit routing control signal.

17. The signal communication system according to claim 16, wherein the routing of a number c of bits of data to the remaining n-c bits that are operable (where c and n are integers such that $1<c<n$) is conducted on a bit by bit basis, k-bit basis, or packet data basis.